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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/658,882 | 09/09/2003 | Kuo-Tung Chang | AMD-H0642 | 3204 |

7590 09/28/2006

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| EXAMINER | |
|---|---|
| LEE, EUGENE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/658,882 | CHANG ET AL. | |
| | Examiner | Art Unit | |
| | Eugene Lee | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *12 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,6-8,11 and 12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-8,11,12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9/12/06 has been entered.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 thru 3, and 6 thru 8, 11, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehrad et al. 6,765,257 B1 in view of Ito et al. 6,700,176 B2. Mehrad discloses (see, for example, FIG. 1) a memory (integrated circuit device) comprising a flash EPROM array (an array of flash memory cells) of memory elements (cells), said memory elements comprising a source, a drain and a stacked gate structure comprising a control gate line (control gate) 15, floating gate (charge trapping layer) 13, insulating layer (see FIG. 2 of Mehrad), horizontal source line (common source line) 17, and source contact 32. The source contact 32 is coupled to the source diffusion. The source contact 32 is coupled to said horizontal

source line 17 wherein the horizontal source line is under the stacked gate structure. The source contact is in the same row as drain contacts 34. Mehrad does not disclose a region under said stacked gate structure comprising overlapping lateral diffusions of implantation regions of said source and said drain. However, Ito discloses (see, for example, FIG. 3) an anti-fuse device 300 comprising overlapping source-drain extension regions 320, 322 wherein an overlapped region 350 exists. The overlapped region is underneath the gate 112. In column 6, lines 46-49, Ito discloses reduced on-state resistance and improved current characteristics. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have a region under said stacked gate structure comprising overlapping lateral diffusions of implantation regions of said source and said drain in order to reduce on-state resistance and improve current characteristics.

Regarding claim 2, see, for example, FIG. 1, wherein Mehrad discloses the control gate line (substantially straight word lines) 15.

Regarding claim 3, see, for example, FIG. 1, wherein Mehrad discloses the horizontal source line 17 having a substantially uniform width.

Regarding claim 6, see, for example, column 1, lines 12-13, wherein Mehrad discloses a FLASH memory array which is non-volatile memory.

Regarding claim 7, see, for example, FIG. 1 wherein Mehrad discloses a floating gate 13.

Regarding claim 8 and the new limitation "wherein dopants are implanted on either sides of said first stacked gate structure, wherein said source and drain implantation regions are able to conduct independent of any voltage applied to said first stacked gate structure", this limitation is a product-by-process limitation of forming the structure of overlapping lateral diffusions of

source and drain implantations regions. Since the claims are directed towards structure (device) and not method of making, the combination of Mehrad in view of Ito still discloses the claimed **structural** limitations.

Regarding claim 11, see, for example, FIG. 2 wherein Mehrad discloses multiple gates (gate and second gate) 13.

Regarding claim 12, see, for example, FIG. 2 wherein Mehrad discloses multiple source contacts (first source contact, and second source contact) 32.

### *Response to Arguments*

4. Applicant's arguments filed 9/12/06 have been fully considered but they are not persuasive.

Regarding the applicant's argument on page 7, first paragraph of the amendment filed 9/12/06 that Mehrad teaches using only "conventional processing", and fails to teach or suggest the possibility or benefit of overlapping the source and drain regions, this argument is not persuasive. It must be recognized that any judgement on obviousness is in any sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the invention was made, and does not include knowledge gleaned only from the Applicant's disclosure, such a reconstruction is proper. In re McLaughlin, 443 F. 2d 1392; 170 USPQ 209 (CCPA1971). In this case, Ito was combined with Mehrad. Such a combination was proper since both references (Ito, and Mehrad) are directed towards non-volatile memories, and since Ito discloses that overlapping the

source/drain regions reduces on-state resistance and improves current characteristics, combining such references would have been obvious to one of ordinary skill in the art.

Regarding the applicant's argument that Ito does not teach a common source line structure, this argument is not persuasive. Mehrad already teaches a common source line and it was not critical that Ito also discloses a common source line since Ito's teaching only involved the overlapping of a source and drain region, and since Ito does not state anything about another region (i.e. common source region) affecting the feasibility of overlapping the source and drain region, such a combination is proper.

## INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
September 20, 2006

EUGENE LEE
PRIMARY EXAMINER